C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - III **CODE**: - 5TE03SMD1
NAME – Semiconductor Memories Design (SMD)

Teaching & Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE03SMD1	Semiconductor Memories Design (SMD)	04	00	02	06	05	30	1.5	70	3.0	--	20	30	150

Objectives: -

- The objective of this course is to provide a systematic and comprehensive insight which aids the understanding of SRAM and DRAM bitcell circuits, architectures, and design and analysis techniques. The nano-regime challenges such as low-power, process variation and soft errors are the core issues considered while designing and analyzing the SRAM and DRAM bitcells in depth.

Prerequisites:

- Students enrolled in this course are expected to have an undergraduate-level equivalent background in the following topics: Logic Circuit Design, Microelectronics, MOSFET Operation, NMOS and PMOS transistors operations and various parameters, MOS-based Logic gates, Sequential Circuits.

Course Outlines:-

Sr. No.	Course Contents
1	**Introduction and Motivation** Motivation, SRAM in the Computer Memory Hierarchy, Technology Scaling and SRAM Design and Test, Moore's Law, Obstacles in SRAM Scaling, SRAM Test Economics, SRAM Design and Test Tradeoffs, Area and Stability, Quality and Yield, Test Coverage and Test Time, Redundancy.
2	**SRAM Circuit Design and Operation** Introduction, SRAM Block Structure, SRAM Cell Design, Four-Transistor (4T) SRAM Cell with Polysilicon Resistor Load, Six-Transistor (6T) CMOS SRAM Cell, Read Operation, Write Operation, Four-Transistor (4T) Loadless SRAM Cell,
3	**The SRAM Array** Sense Amplifier and Bit Line Precharge-Equalization, Write Driver, Row Address Decoder and Column MUX, Address Transition Detector, Timing Control Schemes, Delay-Line Based Timing Control, Replica-Loop Based Timing Control, Pipelined Timing Control
4	**An Introduction to DRAM** DRAM Types and Operation, The 1 k DRAM (First Generation), The 4k-64 Meg DRAM (Second Generation), Synchronous DRAM (Third Generation), DRAM Basics, Access and Sense Operations, Write Operation, Opening a Row (Summary), Open/Folded DRAM Array Architectures.
5	**The DRAM Array** The Mbit Cell, The Sense Amp, Equilibration and Bias Circuits, Isolation Devices, Input / Output Transistors, Nsense and Psense Amplifiers, Rate of Activation, Configurations, Operation, Row

	Decoder Elements, Bootstrap Wordline Driver, NOR Driver, CMOS Driver, Address Decode Tree, Static Tree, P& E Tree, Predecoding, Pass Transistor Tree.
6	**Array Architectures** Array Architectures, Open Digitline Array Architecture, Folded Array Architecture, Design Examples: Advanced Bilevel DRAM Architecture, Array Architecture Objectives, Bilevel Digitline Construction, Bilevel Digitline Array Architecture, and Architectural Comparison.

Learning Outcomes: -

- This course provides a sufficient amount of fundamentals to become familiar with the terminology of the SRAM and DRAM design and analysis.
- The content of this course is directed to nano-scale VLSI and Embedded system design students, who are about to start their research in SRAM and DRAM design.
- It is an important source for students who intended to develop and understand the different aspects of SRAM and DRAM.

Books Recommended:-

1. Andrei Pavlov, Manoj Sachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies", Springer Science + Business Media B.V, 2008.
2. Brent Keeth, R. Jacob Baker, Brian Johnson, Feng Lin, "DRAM Circuit Design-Fundamental and High-Speed Topics" IEEE Press Series on Microelectronic Systems.
3. Jawar Singh, Saraju P.Mohanty and Dhiraj K. Pradhan, "Robust SRAM Designs and Analysis", Springer New York Heidelberg Dordrecht London, 2013.

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - III **CODE**: - 5TE03ELX1
NAME – Embedded Linux (ELX)

Teaching & Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE04ELX1	Embedded Linux (ELX)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives:-

- To study Basics of Linux Operating System
- To study basic Commands of Linux/Unix Operating System
- To study Advanced Linux Concepts used in Embedded Systems Design
- To study Real Time Principles and Challenges in Design of Embedded Linux

Prerequisite:-

- Students should have a firm grasp on basics of Operating Systems and fundamentals of Embedded Systems.

Course Outline:-

Sr. No.	Course Content
1	**Introduction:** History of Embedded Linux, Why Embedded Linux? Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap
2	**The Big Picture:** Embedded or Not?, Anatomy of an Embedded System, Storage Considerations
3	**Processor Basics:** Stand-Alone Processors – IBM 970FX, Intel Pentium M, Intel Atom, Freescale MPC7448, Companion Chips, Integrated Processors: System-on-Chip (SoC) – Power Architecture, Freescale Power Architecture, Freescale PowerQUICC –I, Freescale PowerQUICC-II, PowerQUICC-II Pro, Freescale PowerQUICC-III, Freescale QorIQ, AMCC Power Architecture, MIPS, Broadcom MIPS, ARM, TI ARM, Freescale ARM, Other Architectures
4	**Basic Unix/Linux Commands and Concepts:** Logging In, Setting a Password, Virtual Consoles, Popular Commands, Shells, Useful Keys and How to Get Them to Work, Typing Shortcuts, Filename Expansion, Saving Your Output, What is a Command? Putting a Command in the Background, Remote Logins and Command Execution, Manual Pages, Startup Files, Important Directories, Basic Text Editing, Advanced Shells and Shell Scripting
5	**The Linux Kernel: A Different Perspective:** Background, Linux Kernel Construction, Kernel Build System, Kernel Configuration, Kernel Documentation, Obtaining an Custom Linux Kernel
6	**Kernel Initialization:** Composite Kernel Image: Piggy and Friends, Initialization Flow of Control, Kernel Command-Line Processing, Subsystem Initialization, The init Thread

7	**User Space Initialization:** Root File System, Kernel's Last Boot Steps, The init Process, Initial RAM Disk, Using initramfs
8	**Bootloaders:** Role of a Bootloader, Bootloader Challenges, A Universal Bootloader: U-Boot, Porting U-Boot, Device Tree Blob (Flat Device Tree), Other Bootloaders: Lilo, GRUB
9	**Device Driver Basics:** Device Driver Concepts, Module Utilities, Driver Methods, Bringing It All Together, Building Out-of-Tree Drivers
10	**File Systems :** Linux File System Concepts, ext2, ext3, ext4, ReiserFS, JFFS2, cramfs, Network File System, Pseudo File Systems, Building a Simple File System
11	**MTD Subsystem :** MTD Overview, MTD Partitions, MTD Utilities, UBI File System
12	**Linux and Real Time:** What is Real Time?, Kernel Preemption, Real Time Kernel Patch, Real Time Kernel Performance Analysis

Learning Outcomes:

After the successful completion of the course, students will be able to

- Understand basics of Linux Operating System
- Understand and execute basic commands of Linux Operating Systems
- Understand fundamentals of Linux used in Embedded Systems and Real Time Concepts

Books Recommended:

1. Embedded Linux System Design and Development, P. Raghavan, Amol Lad and Sriram Neelakandan, Auerbach Publications
2. Embedded Linux Primer – A Practical Real World Approach, Christopher Hallinan, Prentice Hall
3. Running Linux, Matthias Kalle Dalheimer and Matt Welsh, O'Relly Publication
4. Embedded Linux: Hardware, Software and Interfacing, Craig Hollabaught, Addison Wesley